IN THE SPECIFICATION:

Please delete the paragraph beginning on Page 3, line 15 and replace with the following new paragraph. Changes from the original paragraph are highlighted.

The problems outlined above may in large part be solved by a method ~~an~~ and apparatus for providing capability information to a shared controller. In one embodiment, a peripheral bus host controller may be shared by a plurality of peripheral devices coupled to a peripheral bus. The peripheral devices may include coder/decoder (codec) circuitry, and may be implemented using a riser card. The host controller may be configured to query the bus for peripheral devices by reading each address on the bus. During the querying process, the host controller may detect one or more peripheral devices coupled to the bus. Following the completion of the querying of the bus, the host controller may then begin reading configuration information from each of the detected devices. The host controller may employ one or more of several different techniques in order to read configuration information from the peripheral device. The configuration information at a minimum includes a device identifier, which may identify the vendor and the function of the device. Additional information needed to configure the device to communicate over the peripheral bus may also be obtained with a read of the device, or various lookup mechanisms, such as a lookup table or a tree-like data structure. After configuration information has been obtained for each device coupled to the bus, the host controller may dynamically configure each of the devices for communication over the bus, thereby allowing the flexibility to enumerate riser cards and add new functions through peripheral devices to the computer system in which the bus is implemented.

Please delete the paragraph beginning on page 8, line 3, and replace with the following new paragraph. Changes from the original paragraph are highlighted.

Turning now to Figure 2, a block diagram of one embodiment of a computer system is shown. Computer system 20 includes a processor 26 coupled to bus interface unit 28 via processor bus 27. Other embodiments, including those having multiple

processors, are possible and contemplated. Bus interface ~~25~~ 28 may be coupled to host controller 24, which may be a host controller for a peripheral bus. In one embodiment, host controller 24 and bus interface 28 may be implemented on the same chip, while other embodiments may implement host controller 24 and bus interface 28 on separate chips. Host controller 24 and bus interface 28 may be coupled by various types of buses, such as a peripheral component interconnect (PCI) bus. Peripheral bus 21 may be a serial bus or a parallel bus. Types of serial buses may include, but are not limited to DSL buses and USB buses. Serial buses may also be based on the AC '97 specification discussed above. Host controller 24 may be coupled to one or more peripheral devices 25 through peripheral bus 21. In the embodiment shown, three peripheral devices are shown coupled to the host controller, although generally speaking, there is no specific upper or lower limit to the number of peripherals that may be coupled to host controller 24.

Please delete the paragraph beginning on page 9, line 22 and completing on page 10, line 9, and replace with the following new paragraph. Changes from the original are highlighted.

Device information read by host controller 24 (or obtained by other means) may be used to configure each of the peripheral devices coupled to the bus and/or the host controller. In some embodiments wherein the peripheral bus is a serial timeslot bus, host controller 24 may obtain information from each peripheral device 25 concerning the assignment of timeslots. Some devices may need a specific quantity of timeslots for communications with the host controller, while other devices may need to be assigned a timeslot in a specific position of a frame (e.g. timeslot 1, timeslot 2, etc.), while some devices may need timeslots in a specific quantity and a specific position. Some embodiments, rather than using timeslots, may conduct communications between host controller 24 and peripheral devices 25 using stream addresses. In such embodiments, host controller 24 may assign a first data stream to a first peripheral device 25, a second data stream to a second peripheral device 25, and so on. Each peripheral device 25 may then monitor peripheral bus 21 for the presence of its assigned data stream. A separate data stream may also be assigned to convey control information between host controller

24 and each of peripheral devices 25. Stream addressing will be discussed in further detail below. Regardless of the type of bus, host controller 24 may determine the data format(s) ~~the~~ that may be required for communications with each of peripheral devices 25.

Please delete the paragraph beginning on page 10, line 17 and replace with the following new paragraph. Changes from the original paragraph are highlighted.

Host controller 24 may also be configured to determine the various modes in which each of peripheral devices 25 may operate. For example, a peripheral device 25 may be a modem, and may be able to operate using various modem protocols, such as V.90 or V.34. The modem may also be configured to operate at various baud rates. ~~This information.~~ Thus, host controller 24 may be configured to determine each protocol and baud rate at which the modem may operate. Similar examples may apply to other peripheral devices that may be coupled to peripheral bus 21. Such peripheral devices may include, but are not limited to CD-ROM players and CD-ROM recorders, DVD-ROM players, network interface cards, sound/audio cards, graphics cards, scanners, printers and printer interfaces, and so forth.

Please delete the paragraph beginning on page 11, line 21 and ending on page 12, line 2, and replace with the following new paragraph. Changes from the original paragraph are highlighted.

Host controller 24 may further utilize serial side bus 29 in order to convey configuration information to each of peripheral devices 25 coupled to peripheral bus 21. For example, host controller 24 may convey information to each peripheral device 25 concerning their assigned timeslots or stream addresses. Host controller 24 may also utilize serial side bus 29 in order to write configuration information for each device into serial EPROM 31, which may then store the configuration information. Serial EPROM 31 may be accessed by host controller 24 and/or peripheral devices 25 in order to read

configuration information if necessary. Host controller 24 may also perform additional writes to serial EPROM ~~24~~ 31 if there is a change in the status of one or more devices coupled to the bus.

Please delete the paragraph beginning on page 12, line 4, and replace with the following new paragraph. Changes from the original paragraph are highlighted.

Computer system 20 may be configured for plug and play devices. Peripheral bus 21 may be configured to allow plug and play compatible devices to be added subsequent to the initial configuring of peripheral bus 21. Host controller 24 may be configured to detect the addition of a plug and play device. Responsive to the detection of an added plug an play device, host controller 24 may reconfigure the bus, as well as each peripheral device 25 already coupled to the bus. For example, host controller 24 may be configured to change the timeslot assignments for one or more devices or stream addressing requirements for one or more devices. Host controller 24 may also reconfigure I/O address space assignments based on the detection of a new device. Host controller 24 may further be able to resolve conflicts between the various peripheral devices 25, such as conflicts between devices concerning timeslot assignments, stream address assignments, interrupt requests, and so on. This may allow host controller 24 to easily reconfigure peripheral bus 21 at any time subsequent to its initial configuration in order to allow a multitude of new devices to operate with computer system 20.

Please delete the paragraph beginning on page 19, line 13, and replace with the following new paragraph. Changes from the original paragraph are highlighted.

After reading device identification information and obtaining configuration information, the host controller may then begin configuring the peripheral bus. This may include the assignment of timeslots or stream addresses (Step 208). The assignment of timeslots or stream addresses for each peripheral device may be ~~base~~ based upon many different factors, such as bandwidth requirements, data formats, and so forth. Configuring the peripheral bus may also include preparing each device, as well as the

host controller, for certain modes of operation. For example, the host controller may determine whether a particular peripheral device is to operate in a single-pin mode or a dual-pin mode on a DSL bus, or may determine an audio mode for a device operating under the AC '97 specification.